In the Office Action, claims 16-21 and 25-28 are rejected under 35 U.S.C. 102(e), claims 22-24 and 29-31 are rejected under 35 U.S.C. 103(a), and claims 22-24 are objected to. In response, Applicants are amending the Application and claim 22 to correct informalities, canceling claims 17 and 26, and adding new claims 38-40. After entry of the foregoing amendments, claims 16, 18-25, 27-31, and 38-40 are pending in the Application. No new subject matter has been added to the Application. Reconsideration and allowance of the Application in view of the present amendments and remarks is respectfully requested.

Amendments to the Application

Applicants are amending paragraph [0021] on page 7 of the Application to correct typographical errors. Specifically, Applicants are correcting the reference numerals for the "System Memory" and the "System Bus."

Claim Objections

On page 2 of the Office Action, claims 22-24 are objected to because of informalities. Concerning claim 22, the Examiner states that the expression "so that" should be replaced with the term "wherein" to better define the synchronization function of the controller. In response, Applicants are amending claim 22 to replace the expression "so that" with the term "and." Applicants assert that the objection to claim 22 has been overcome and should be withdrawn. Claims 23 and 24 each depend directly from claim 22 and are allowable for the same reasons set forth above for claim 22.

<u>Rejection of Claims 16-21 and 25-28 under 35 U.S.C. 102(e)</u>

On page 3 of the Office Action, claims 16-21 and 25-28 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,054,121 to Koschella (hereinafter, <u>Koschella</u>). In response, Applicants are canceling claims 17 and 26, and amending each of independent claims 16 and 25 to recite a "non-volatile memory." In contrast to each of claims 16 and 25, <u>Koschella</u> does not teach the use of a non-volatile memory. Instead, <u>Koschella</u> discloses a protection circuit that operates with a processor and a "memory device." Further, Applicants find no motivation or suggestion in <u>Koschella</u> for using a non-volatile memory. <u>Koschella</u> does not even mention a non-volatile memory. Because Koschella does not teach does not teach or suggest all the claim limitations of each of independent claims 16 and 25, Applicants assert that the each of independent claims 16 and 25 is allowable. Each of claims 18-24 depends either directly or indirectly from claim 16 and is allowable for the same reasons set forth above for claim 16. Each of claims 27-31 depends either directly or indirectly from claim 25 and is allowable for the same reasons set forth above for claim 25.

Additionally, Applicants are amending independent claim 16 to require logic configured to authorize software to run on a CPU. As amended, claim 16 now recites "a controller configured to allow JTAG hardware to write information into said protected area through said JTAG interface, and allow said logic exclusive access to read said written information, said logic configured to authorize software to run on a CPU based on said written information." In contrast to claim 16, <u>Koschella</u> does not teach or suggest such a structure or combination of structure.

As Applicants understand the invention disclosed in <u>Koschella</u>, a protection circuit allows a processor to access individual memory areas each having a predetermined size in a memory device. As Applicants further understand the invention disclosed in <u>Koschella</u>, a memory protection control register holds individual access authorizations for the memory areas. Unlike the invention disclosed in <u>Koschella</u>, claim 16 requires a controller configured to allow JTAG hardware to write information into a protected area of a non-volatile memory through a JTAG interface and allow logic exclusive access to read the written information. Further, claim 16 requires that the logic be configured to authorize software to run on a CPU based on the written information.

Applicants assert that the invention claimed in claim 16 performs a different function than the invention disclosed in Koschella. In particular, Koschella discloses using a memory protection control register to authorize access to individual memory areas having a predetermined size in a memory device. In contrast to Koschella, claim 16 requires logic configured to authorize software to run on a CPU based on written information in a protected area of a non-volatile memory. Moreover, claim 16 does not require such software to be stored in the non-volatile memory.

For all the above reasons, Applicants assert that Koschella does not teach or suggest each and every claim limitation of claim 16, and thus claim 16 is allowable. Each of dependent claims 18-24 depends either directly or indirectly from claim 16 and is allowable for the same reasons set forth above for claim 16.

Further concerning claim 25, Koschella does not teach or suggest a controller that is clocked either by a system clock signal or by a JTAG clock signal if the system clock signal is not available, as is required in claim 25. Koschella discloses an opcode fetch signal (OPC), a read enable signal (RE), and a write enable signal (WE), which are provided by a CPU to clock a logic device. Further, Koschella discloses a "JTAG" signal and a "TEST" signal for activating a data interface. Unlike claim 25, Koschella does not disclose a system clock signal or a JTAG clock signal. Further, Koschella does not teach or suggest using a JTAG clock signal if a system clock signal is not available. Because Koschella does not teach or suggest each and every claim limitation of claim 25, Applicants assert that claim 25 is allowable. Each of dependent claims 27-31 depends either directly or indirectly from claim 25 and is allowable for the same reasons set forth above for claim 25.

Rejection of Claims 22-24 and 29-31 under 35 U.S.C. 103(a)

On page 5 of the Office Action, claims 22-24 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koschella in view of U.S. Patent No. 6,671,841 to Golshan (hereinafter, Golshan). Each of claim 22-24 depends indirectly from claim 16 and is allowable for the same reasons set forth above for claim 16 in the section entitled "Rejection of Claims 16-21 and 25-28 under 35 U.S.C. 102(b)." Each of claim 29-31 depends indirectly from claim 25 and is allowable for the same reasons set forth

above for claim 25 in the section entitled "Rejection of Claims 16-21 and 25-28 under 35 U.S.C. 102(e)."

Further concerning the rejection of claims 22-24 and 29-31 under 35 U.S.C. 103(a), the Examiner states on page 5 of the Office Action that Golshan discloses a synchronizer for synchronizing a JTAG clock to a system clock CPU clock. The Examiner further states on pages 5-6 of the Office Action that "[i]t would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a synchronizer as taught by Golshan, in the processor-memory of Koschella, for eliminating clock skewing associated with asynchronous clocks." Unlike Golshan, each of claims 22 and 29 do not require synchronizing a JTAG clock to a system clock.

Claim 22 requires at least one synchronization buffer to synchronize communications received from a CPU interface and a JTAG interface. Claim 29 requires a synchronization buffer for synchronizing signals between a JTAG interface and a controller when the controller is clocked by a system clock signal. One advantage of using a synchronization buffer to synchronize communications or signals is that a JTAG clock need not be synchronized to a system clock. Stated differently, the JTAG clock and the system clock may operate asynchronously with respect to each other. In contrast to each of claims 22 and 29, Golshan does not teach or suggest a synchronization buffer or using a synchronization buffer to synchronize communications or signals. Because Golshan and Koschella, either individually or in combination, do not teach or suggest each and every limitation in each of claims 22 and 29, Applicants assert that each of claims 22 and 29 is allowable. Each of claims 23 and 24 depends directly from claim 22 and is allowable for the same reasons set forth above for claim 22. Each of claims 30 and 31 depends either directly or indirectly from claim 29 and is allowable for the same reasons set forth above for claim 29.

Applicants are adding new dependent claims 38-40 to focus on particular embodiments of the invention disclosed in the Application. Each of claims 38 and 39 depends from independent claim 16. Claim 40 depends from independent claim 25.

Each of dependent claims 38 and 40 recites "a reset circuit coupled to said controller and a plurality of external boot configuration vector pins, wherein said reset circuit generates one or more initialization signals upon activation using said first boot configuration vector if a status of a designated one of said plurality of external boot configuration vector pins is a first state or using a second boot configuration vector provided on others of said plurality of external boot configuration pins if the status of said designated one of said external boot configuration vector pins is a second state." Koschella and Golshan, either individually or in combination, do not teach or suggest such a structure or combination of structure. Because Golshan and Koschella, either individually or in combination, do not teach or suggest each and every limitation in each of claims 38 and 40, Applicants assert that each of claims 38 and 40 is allowable.

Dependent claim 39 recites "said written information comprises an authorization unit information block and an authorization unit information block pointer, said authorization unit information block comprises secret information for authorizing said software, said authorization unit information block pointer is configured to specify an initial address of said authorization unit information block, and said logic is further configured to lock said software to said CPU." Koschella and Golshan, either individually or in combination, do not teach or suggest such a structure or combination of structure. Because Golshan and Koschella, either individually or in combination, do not teach or suggest each and every limitation in claim 39, Applicants assert that claim 39 is allowable.

Cited References

In the Office Action, the Examiner cites and relies upon U.S. Patent No. 6,671,841 to Golshan. Applicants request that this reference be added to the Notice of References Cited in the Office Action.

In the Notice of References Cited, the Examiner lists U.S. Patent No. 6,751,764 to Golshan et al., U.S. Patent No. 7,133,990 to Link et al., and U.S. Patent Pub. No. 2006/0294059 to Chamberlain et al., but does not cite or rely upon any of these references in rejecting claims in the Office Action. Applicants duly note these references.

<div align="center">CONCLUSION</div>

Applicants respectfully request reconsideration of the Application based on the amendments and remarks presented above. In light of the above amendments and remarks, Applicants respectfully assert that the claims now pending in the Application are in condition for allowance.

Applicants have made a diligent effort to place the claims in condition for allowance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' representative, Kenneth Glass, at (408) 354-4448 so that such issues may be resolved as expeditiously as possible.

For the reasons set forth in this paper, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

_____4/27/07_____　　　　　_____/Kenneth Glass/_____
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